FIG.1

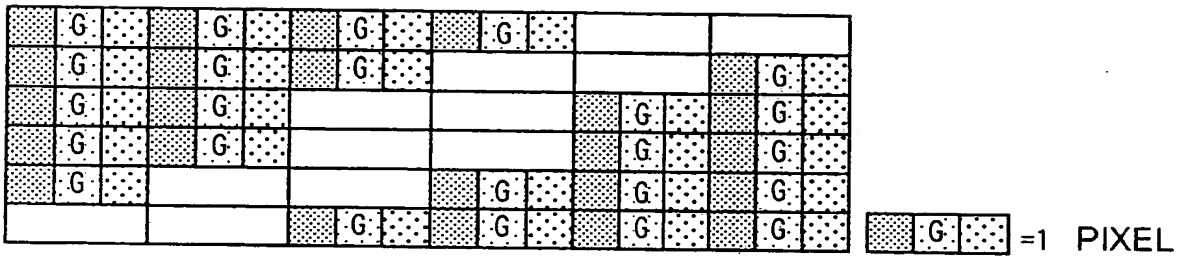


FIG.2

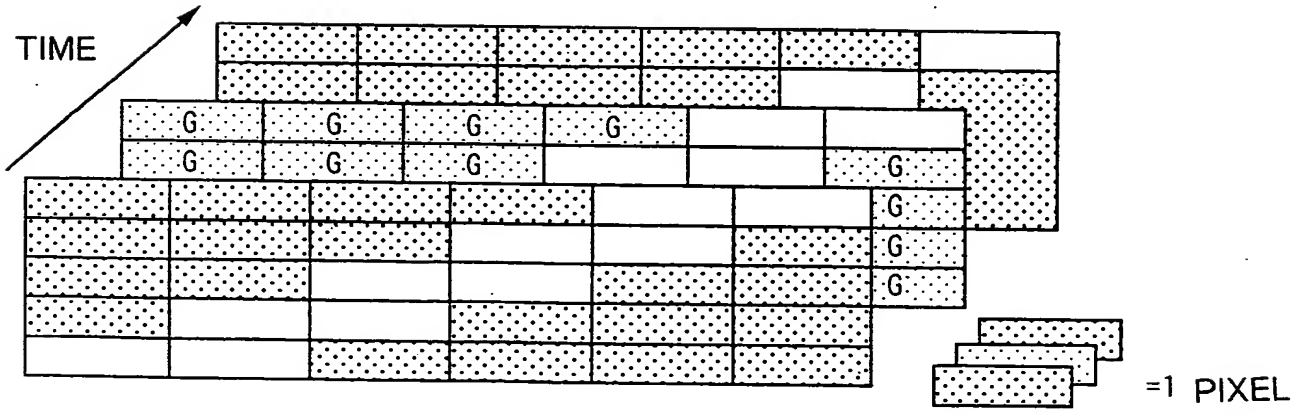


FIG.3

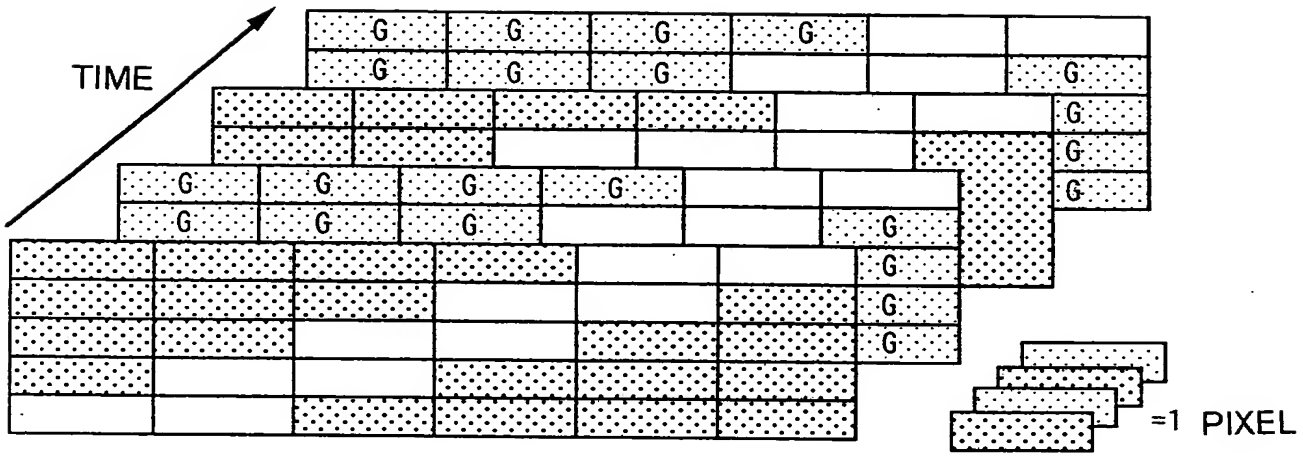


FIG.4A

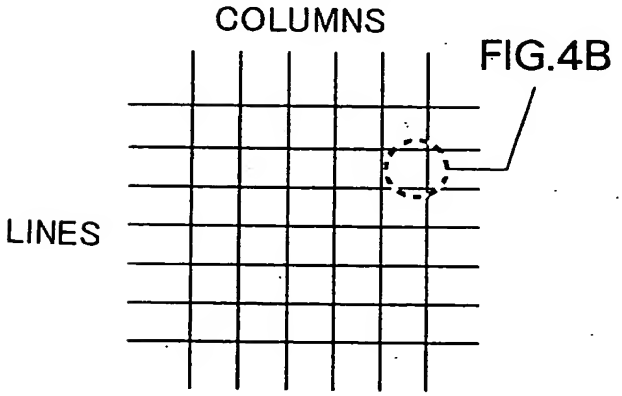

COLUMNS
FIG.4B
LINES

FIG.4B

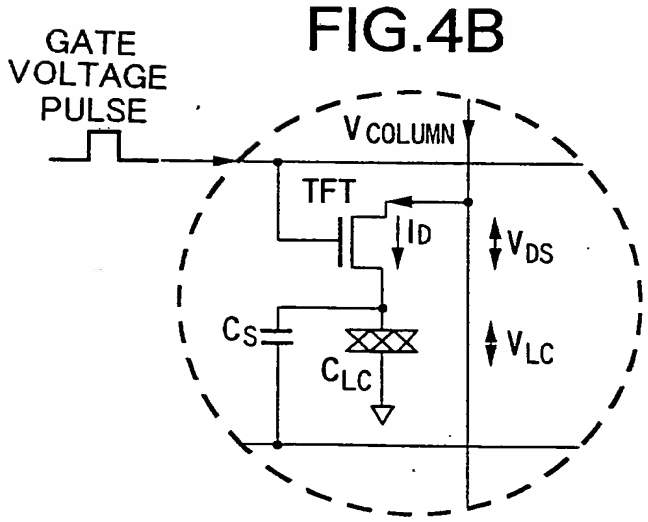

GATE
VOLTAGE
PULSE
V COLUMN
TFT
ID
VDS
CS
CLC
VLC

FIG.5

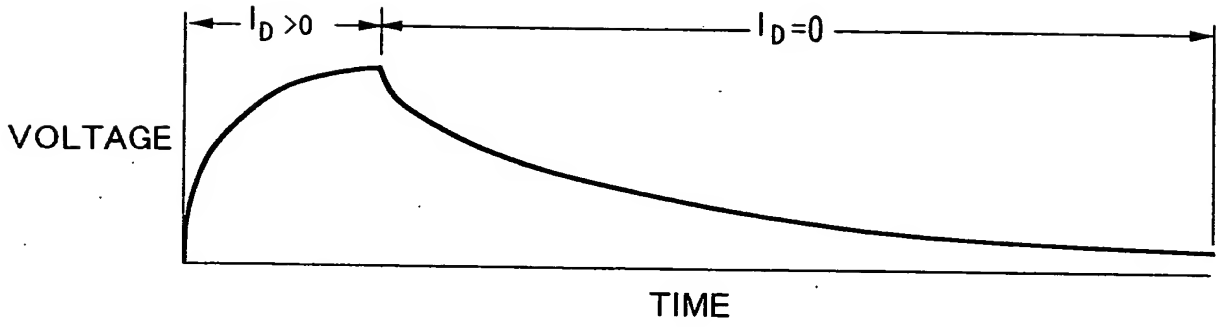


FIG.6

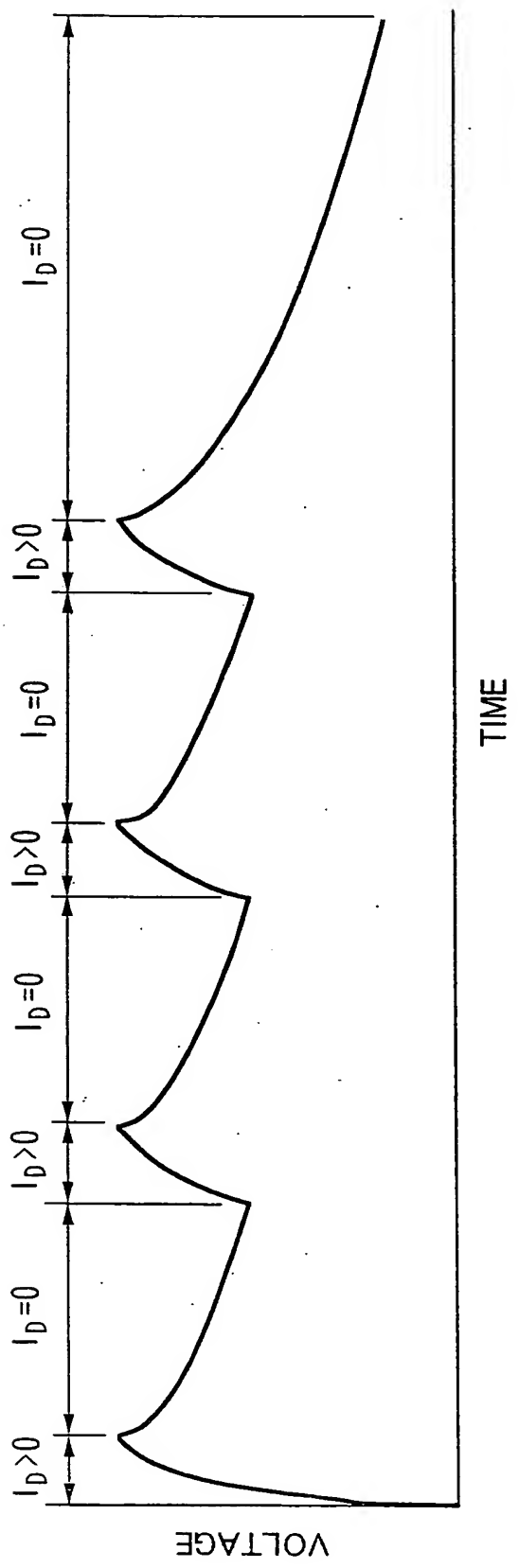


FIG.7

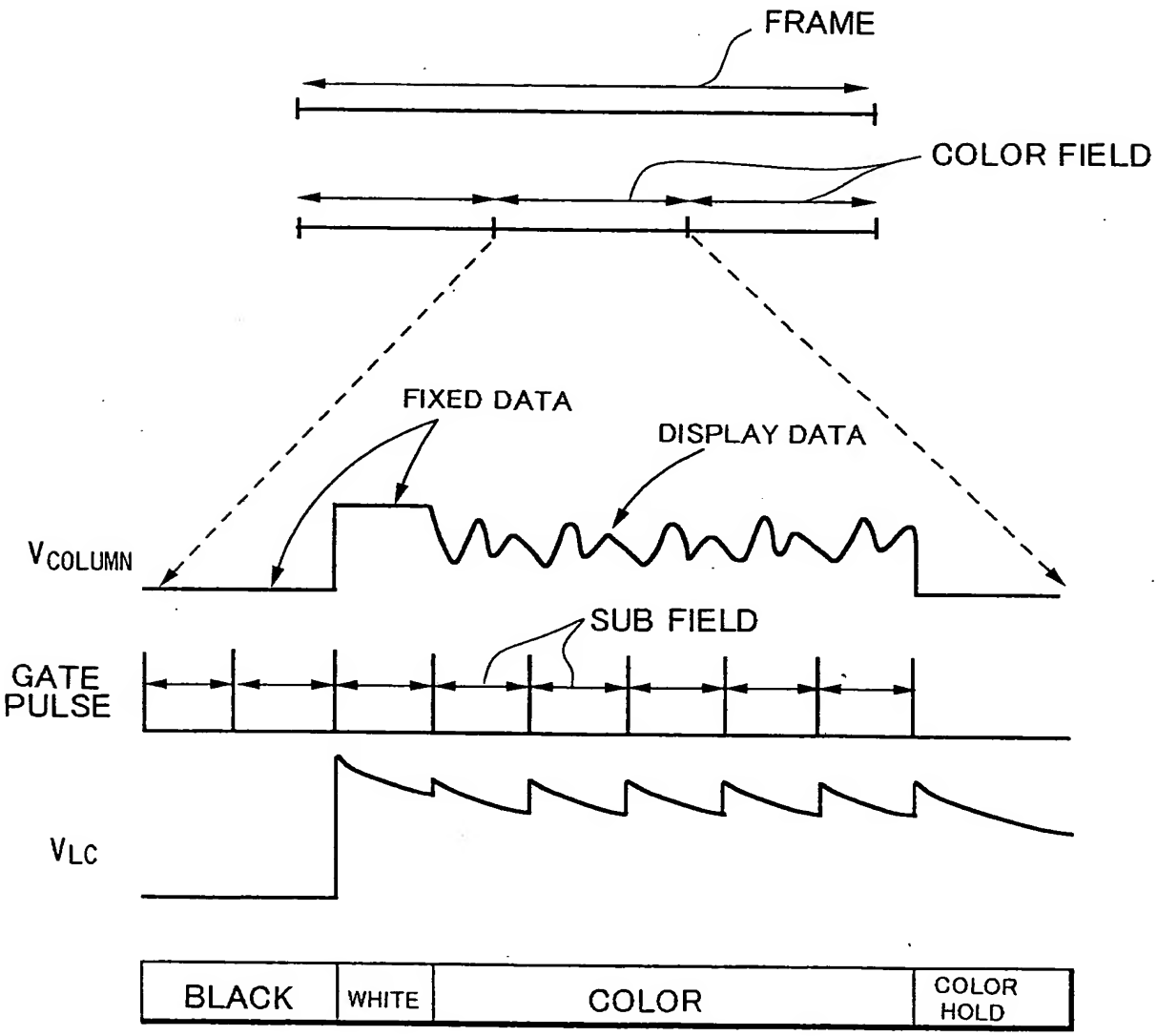

FRAME
COLOR FIELD
FIXED DATA
DISPLAY DATA
VCOLUMN
SUB FIELD
GATE PULSE
VLC
BLACK
WHITE
COLOR
COLOR HOLD

FIG.8

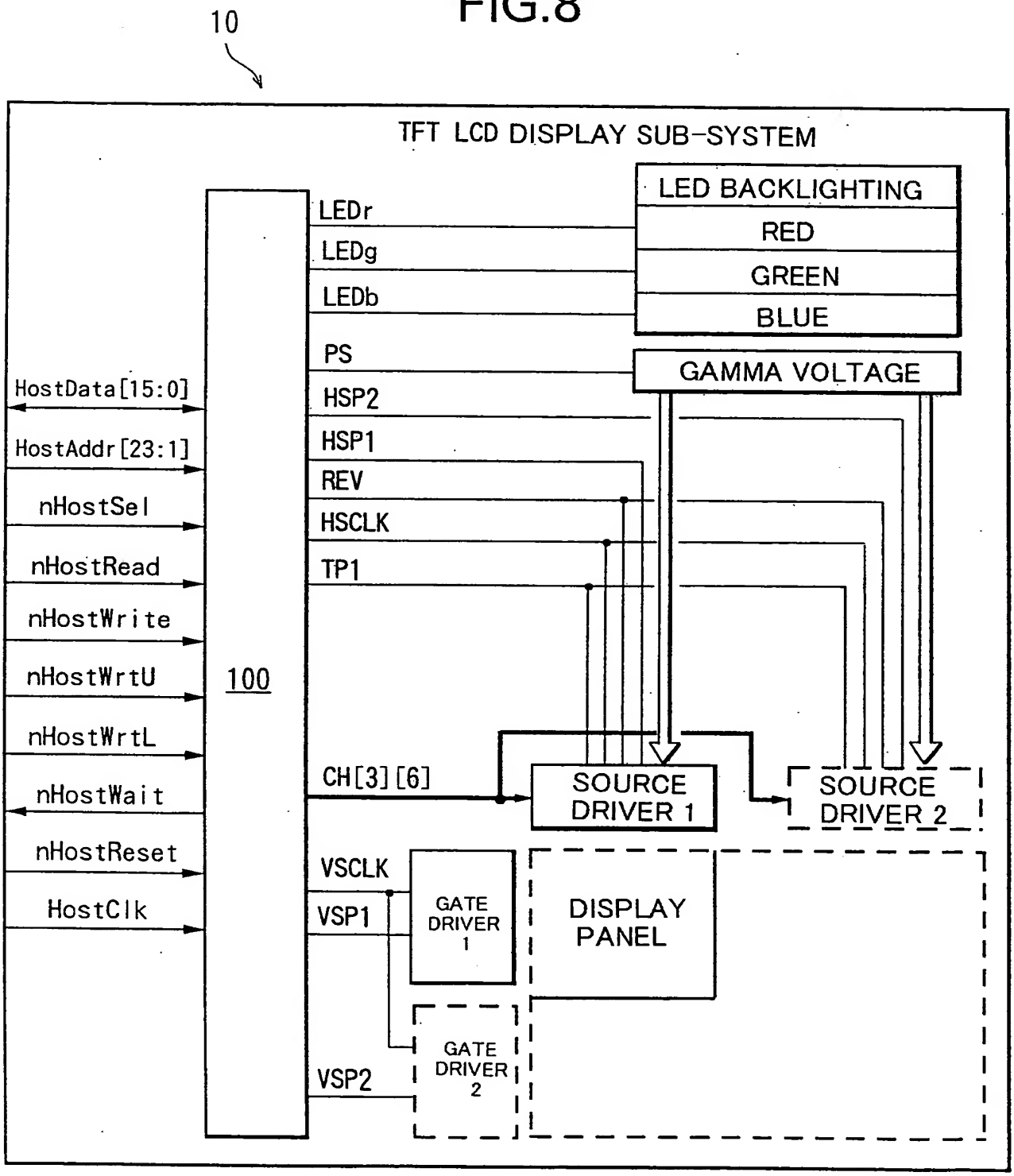

10
TFT LCD DISPLAY SUB-SYSTEM
LED BACKLIGHTING
RED
GREEN
BLUE
GAMMA VOLTAGE
LEDr
LEDg
LEDb
PS
HSP2
HSP1
REV
HSCLK
TP1
HostData[15:0]
HostAddr[23:1]
nHostSel
nHostRead
nHostWrite
nHostWrtU
nHostWrtL
nHostWait
nHostReset
HostClk
100
CH[3][6]
SOURCE DRIVER 1
SOURCE DRIVER 2
VSCLK
VSP1
VSP2
GATE DRIVER 1
GATE DRIVER 2
DISPLAY PANEL

FIG.9

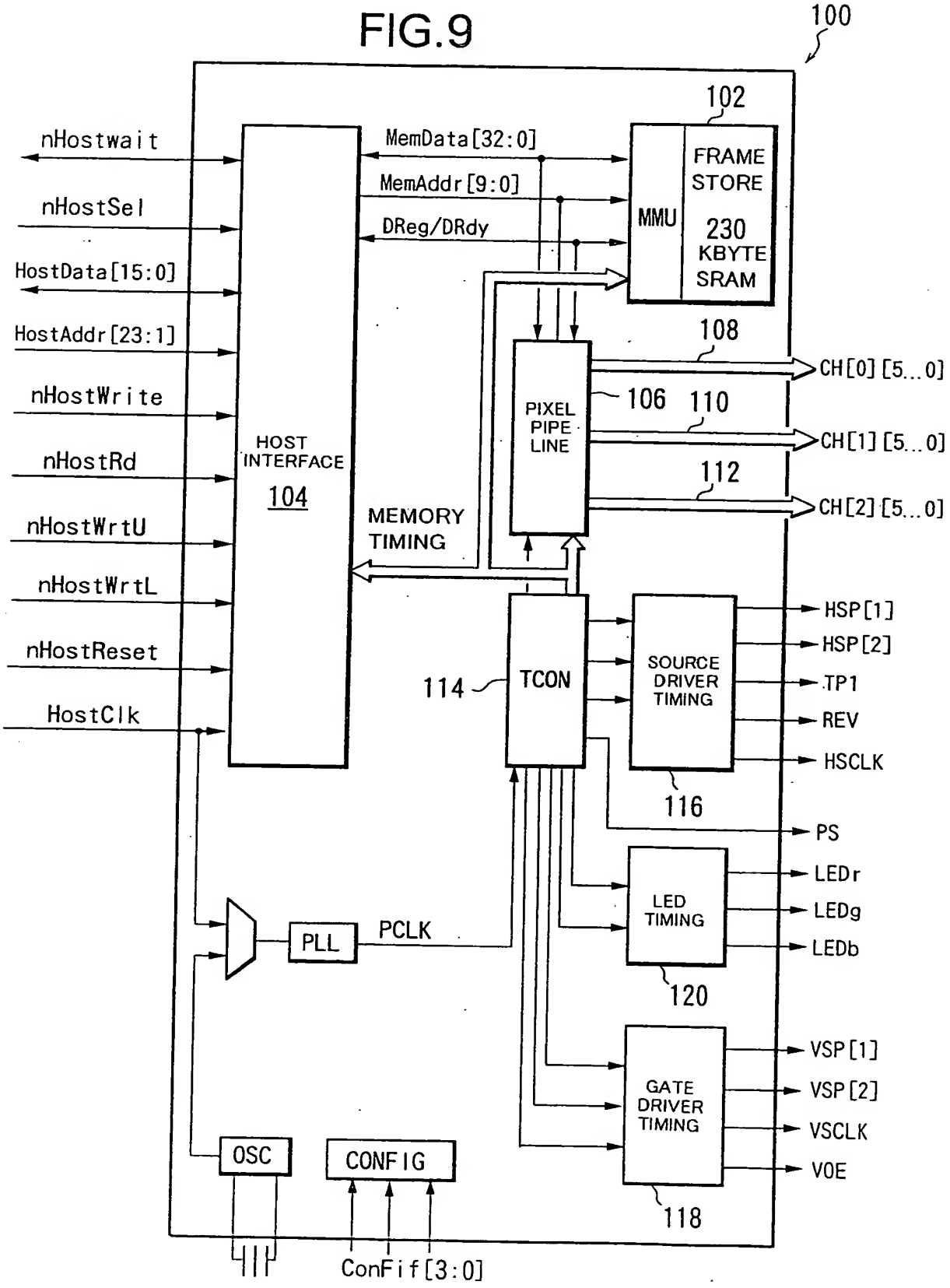

100
102
nHostwait
nHostSel
HostData[15:0]
HostAddr[23:1]
nHostWrite
nHostRd
nHostWrtU
nHostWrtL
nHostReset
HostClk
MemData[32:0]
MemAddr[9:0]
DReg/DRdy
MMU
FRAME STORE
230 KBYTE SRAM
HOST INTERFACE
104
MEMORY TIMING
108
106
110
112
PIXEL PIPE LINE
CH[0][5...0]
CH[1][5...0]
CH[2][5...0]
114
TCON
SOURCE DRIVER TIMING
HSP[1]
HSP[2]
TP1
REV
HSCLK
116
PS
LED TIMING
LEDr
LEDg
LEDb
120
PLL
PCLK
GATE DRIVER TIMING
VSP[1]
VSP[2]
VSCLK
VOE
118
OSC
CONFIG
ConFif[3:0]

FIG.10A

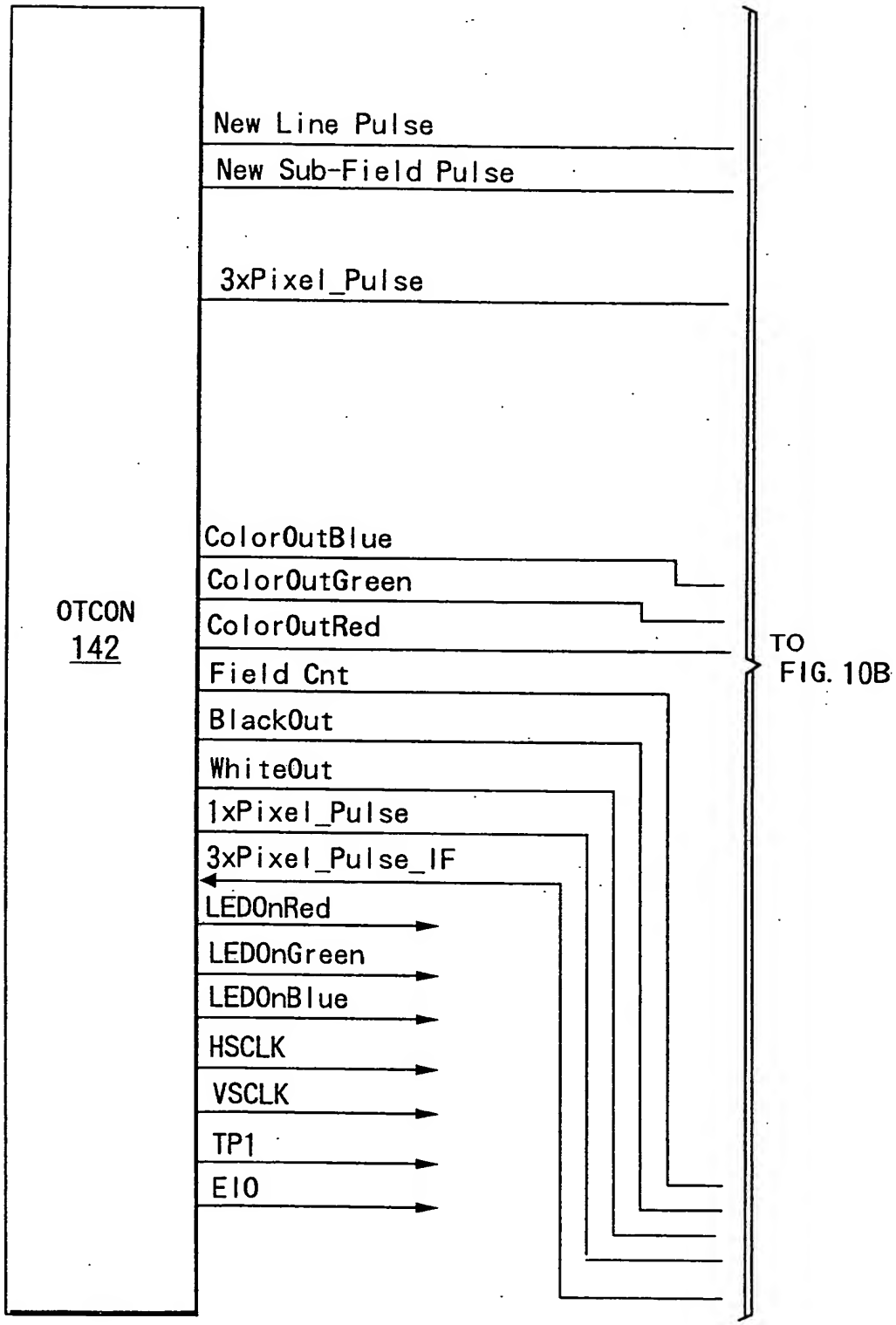

OTCON
142
New Line Pulse
New Sub-Field Pulse
3xPixel_Pulse
ColorOutBlue
ColorOutGreen
ColorOutRed
Field Cnt
BlackOut
WhiteOut
1xPixel_Pulse
3xPixel_Pulse_IF
LEDOnRed
LEDOnGreen
LEDOnBlue
HSCLK
VSCLK
TP1
EIO
TO
FIG. 10B

FIG.10B

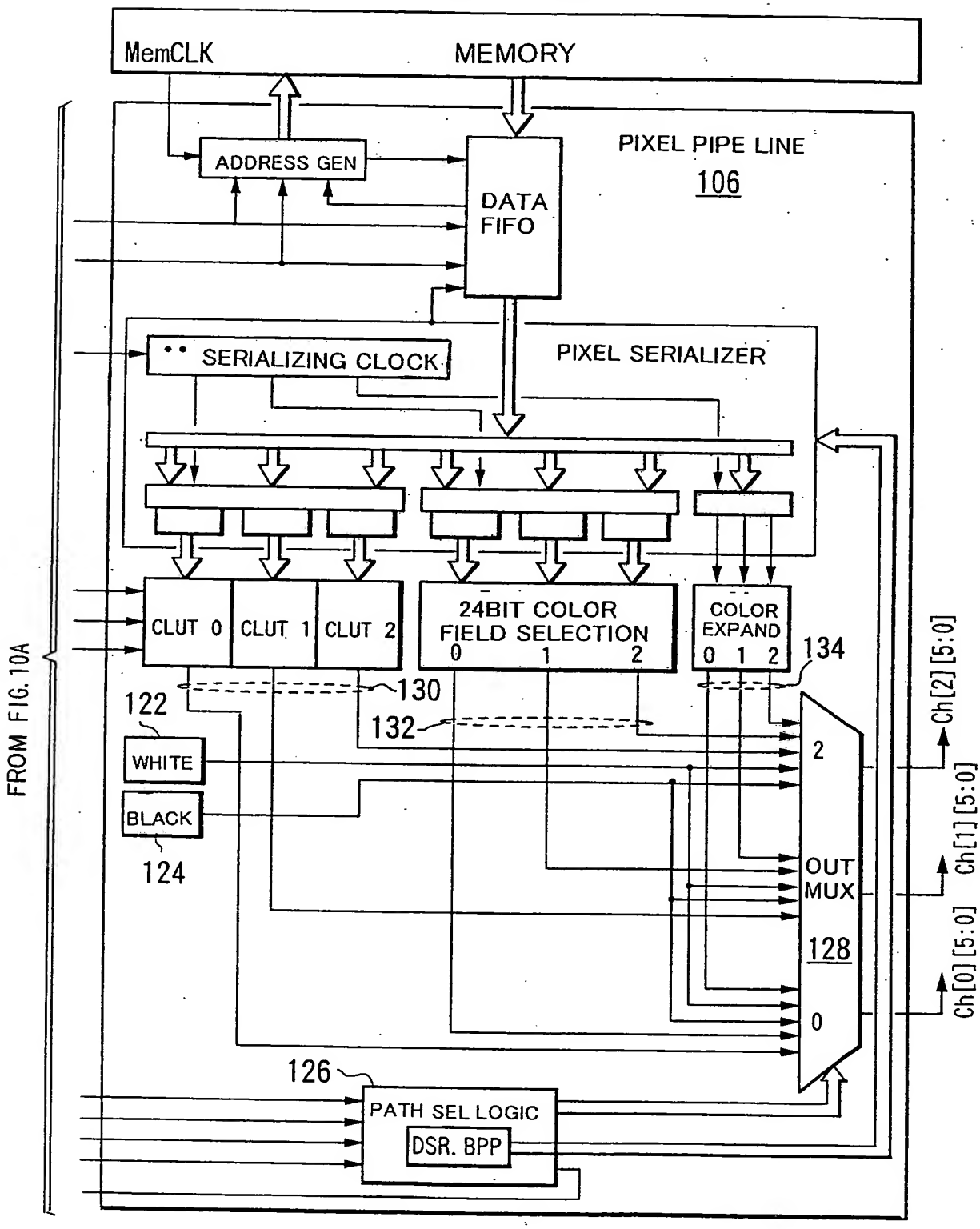

MemCLK
MEMORY
ADDRESS GEN
DATA FIFO
PIXEL PIPE LINE
106
SERIALIZING CLOCK
PIXEL SERIALIZER
CLUT 0
CLUT 1
CLUT 2
24BIT COLOR FIELD SELECTION
0 1 2
COLOR EXPAND
0 1 2
134
130
122
132
WHITE
BLACK
124
2
OUT MUX
128
0
126
PATH SEL LOGIC
DSR. BPP
FROM FIG. 10A
Ch[2] [5:0]
Ch[1] [5:0]
Ch[0] [5:0]

FIG.11

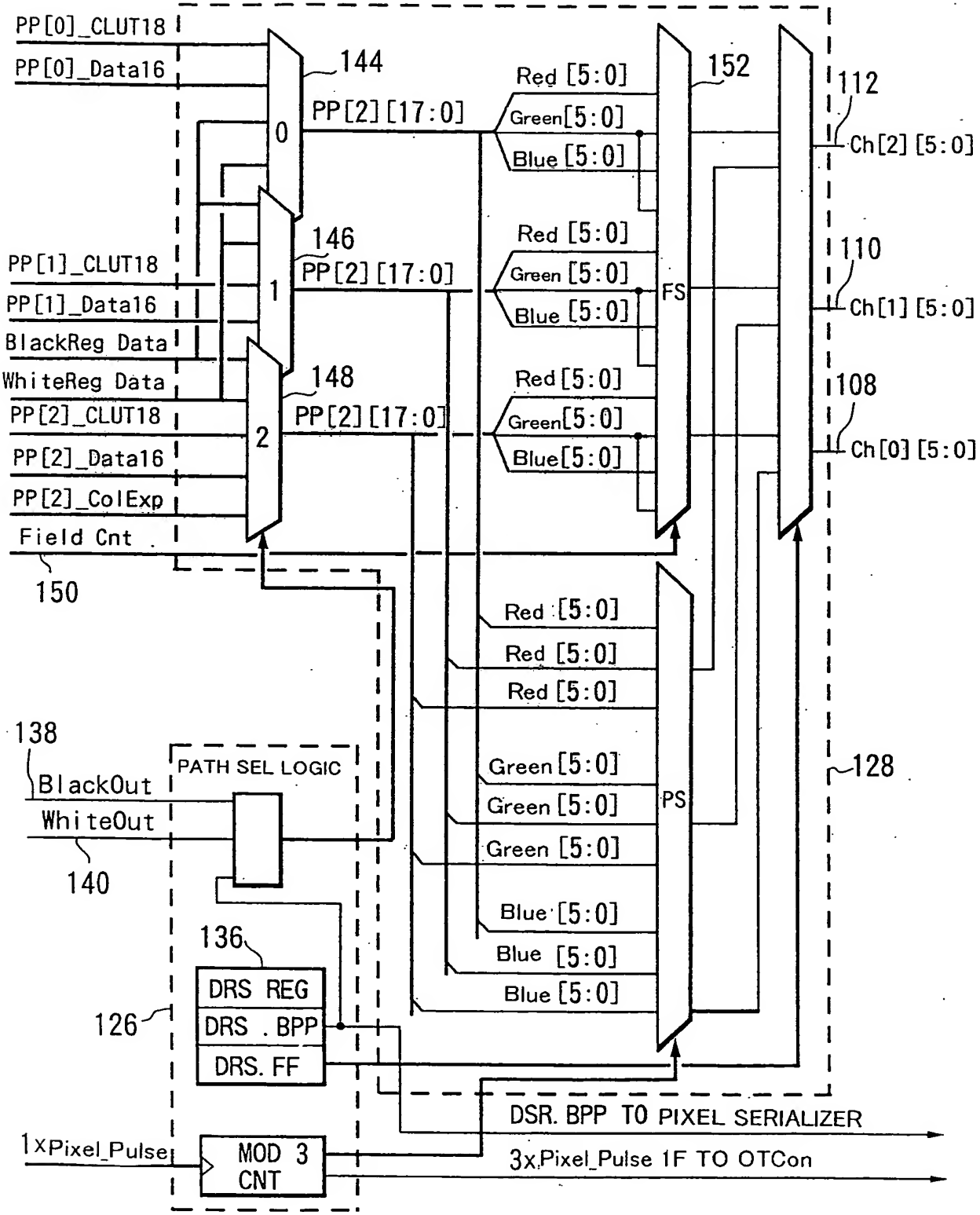
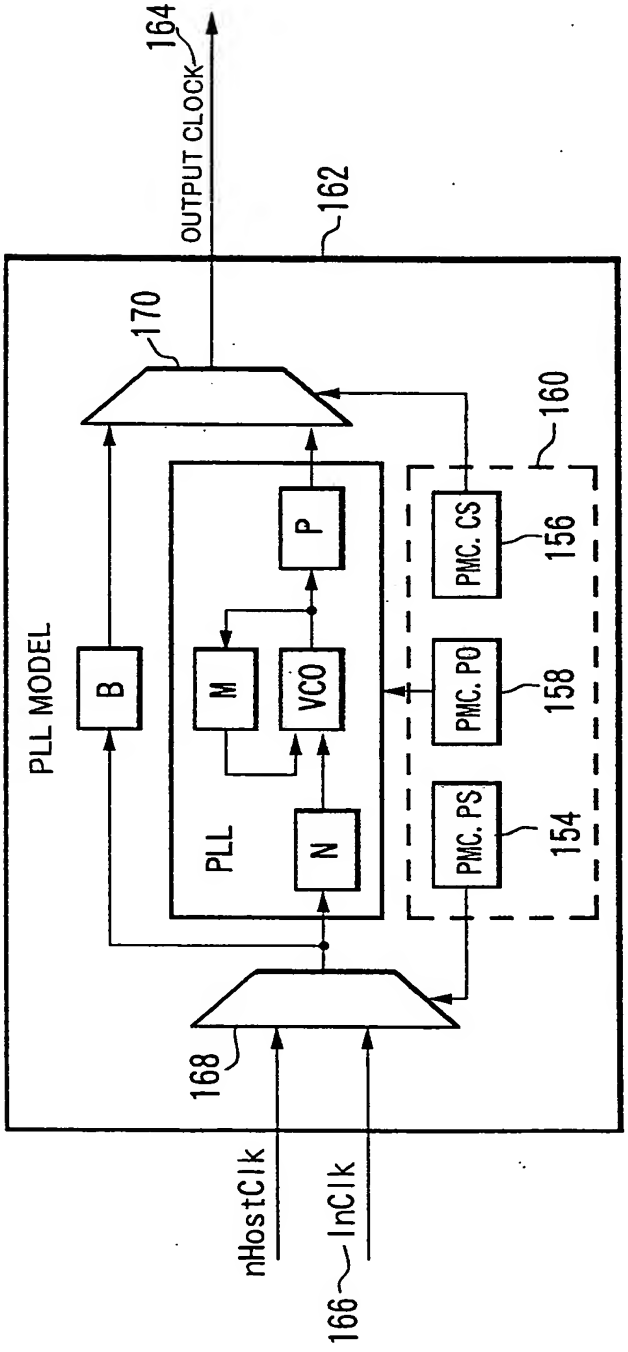

PP[0]_CLUT18
PP[0]_Data16
144
PP[2][17:0]
Red [5:0]
Green[5:0]
Blue [5:0]
152
112
Ch[2] [5:0]
PP[1]_CLUT18
PP[1]_Data16
BlackReg Data
WhiteReg Data
PP[2]_CLUT18
PP[2]_Data16
PP[2]_ColExp
Field Cnt
146
148
FS
110
Ch[1] [5:0]
108
Ch[0] [5:0]
150
PS
128
138
BlackOut
WhiteOut
140
PATH SEL LOGIC
136
126
DRS REG
DRS . BPP
DRS. FF
DSR. BPP TO PIXEL SERIALIZER
1xPixel_Pulse
MOD 3 CNT
3xPixel_Pulse 1F TO OTCon

FIG.12


164
OUTPUT CLOCK
162
170
160
PLL MODEL
B
M
VCO
P
PLL
N
PMC. CS
156
PMC. PO
158
PMC. PS
154
168
nHostClk
InClk
166

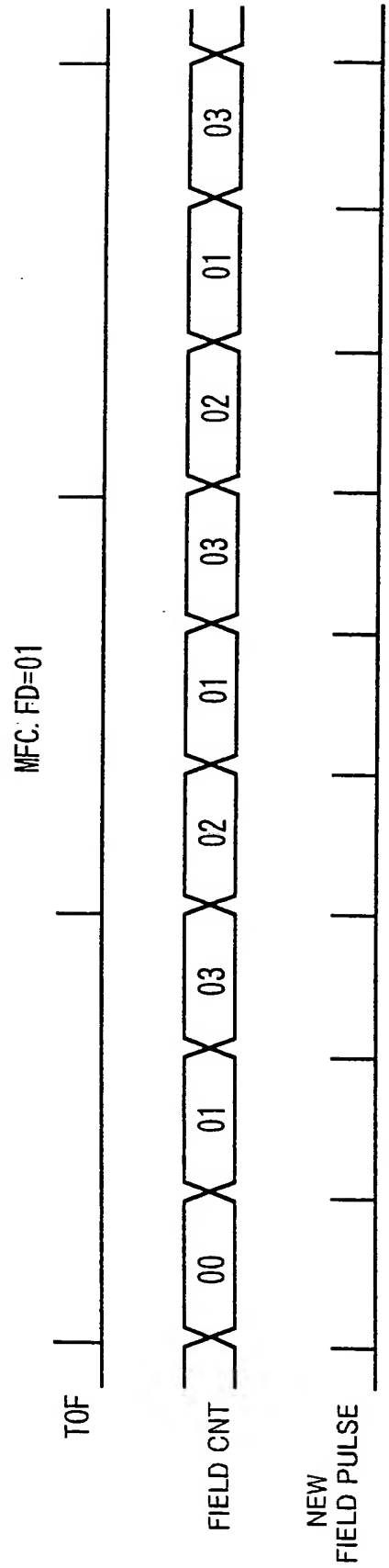


FIG.13A

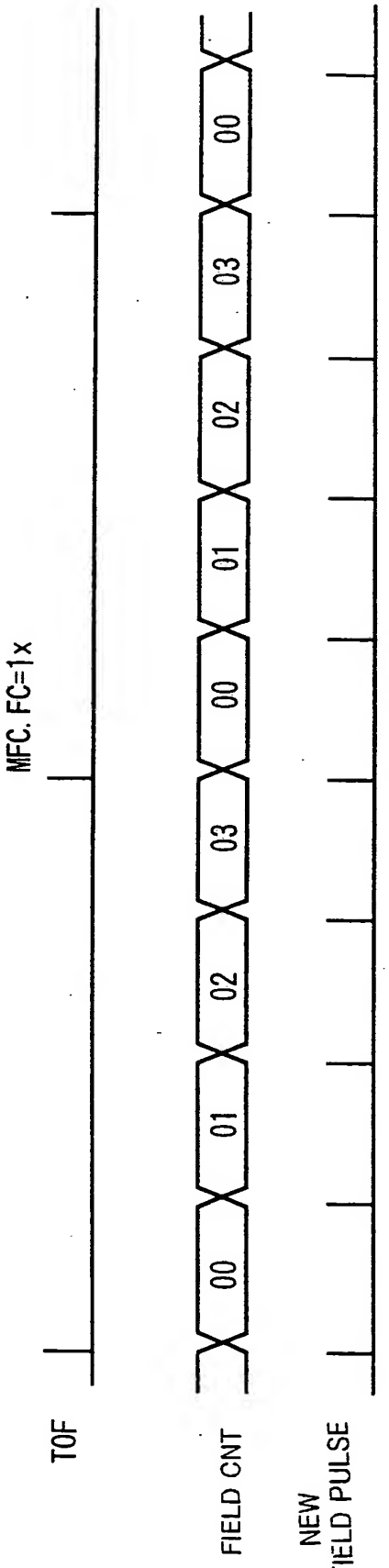


FIG.13B

FIG.14

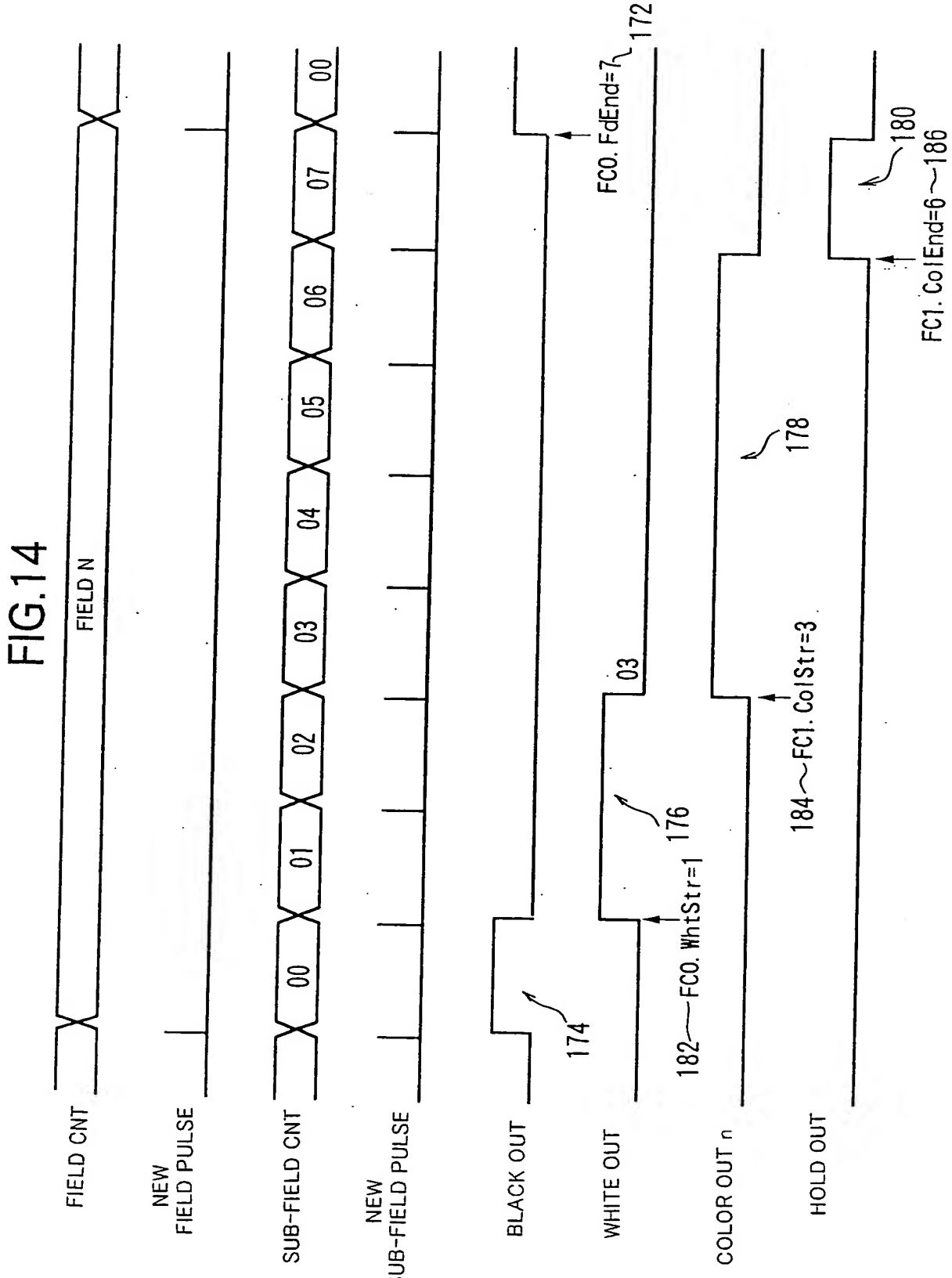

FIELD CNT
FIELD N
NEW FIELD PULSE
SUB-FIELD CNT
00
01
02
03
04
05
06
07
00
NEW SUB-FIELD PULSE
BLACK OUT
174
FC0. FdEnd=7
172
WHITE OUT
03
176
182
FC0. WhtStr=1
COLOR OUT n
178
184
FC1. ColStr=3
HOLD OUT
180
FC1. ColEnd=6~186

FIG.15

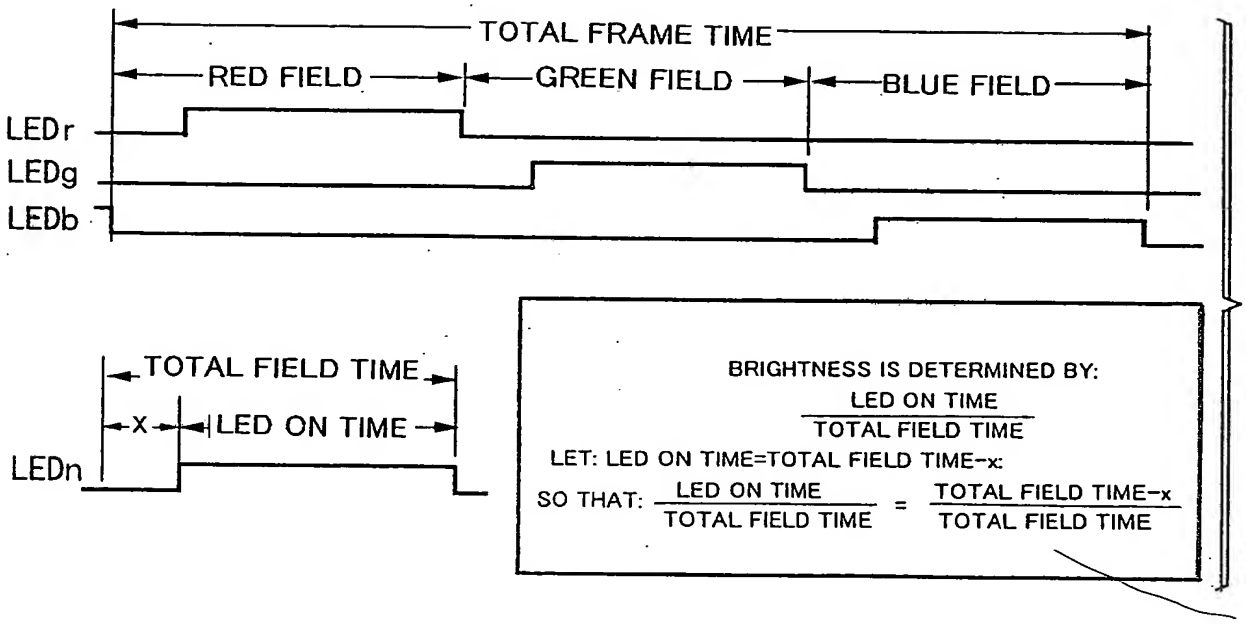

TOTAL FRAME TIME
RED FIELD
GREEN FIELD
BLUE FIELD
LEDr
LEDg
LEDb
TOTAL FIELD TIME
x
LED ON TIME
LEDn
BRIGHTNESS IS DETERMINED BY:
LED ON TIME / TOTAL FIELD TIME
LET: LED ON TIME=TOTAL FIELD TIME-x:
SO THAT: LED ON TIME / TOTAL FIELD TIME = TOTAL FIELD TIME-x / TOTAL FIELD TIME

FIG.16

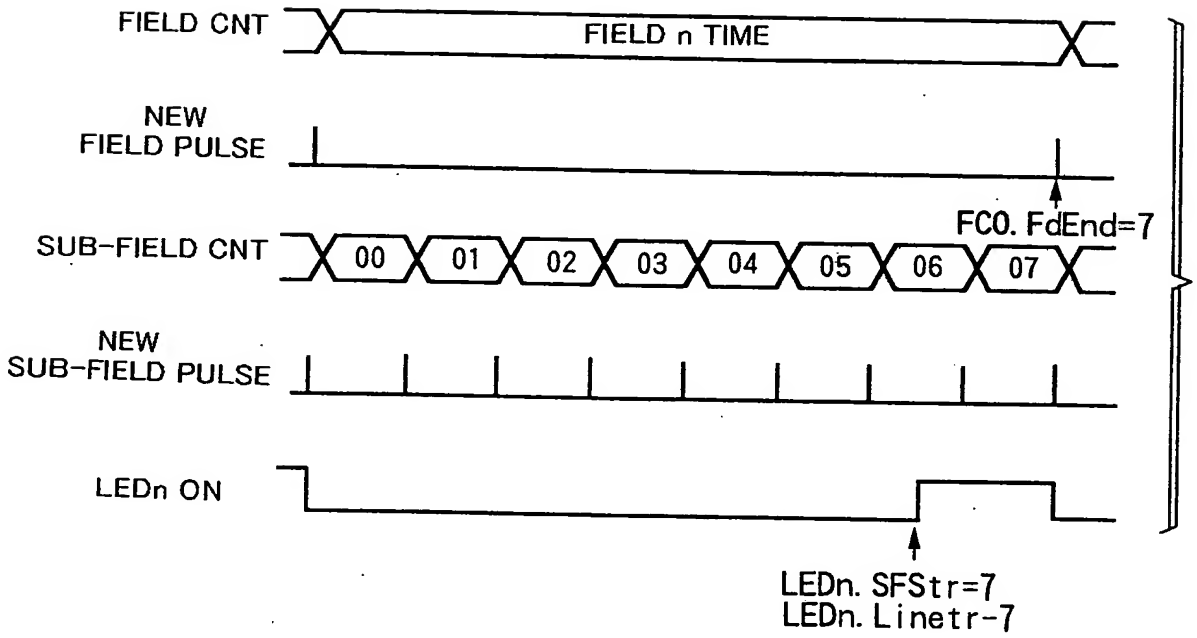

FIELD CNT
FIELD n TIME
NEW
FIELD PULSE
FCO. FdEnd=7
SUB-FIELD CNT
00
01
02
03
04
05
06
07
NEW
SUB-FIELD PULSE
LEDn ON
LEDn. SFStr=7
LEDn. Linetr-7

FIG.17

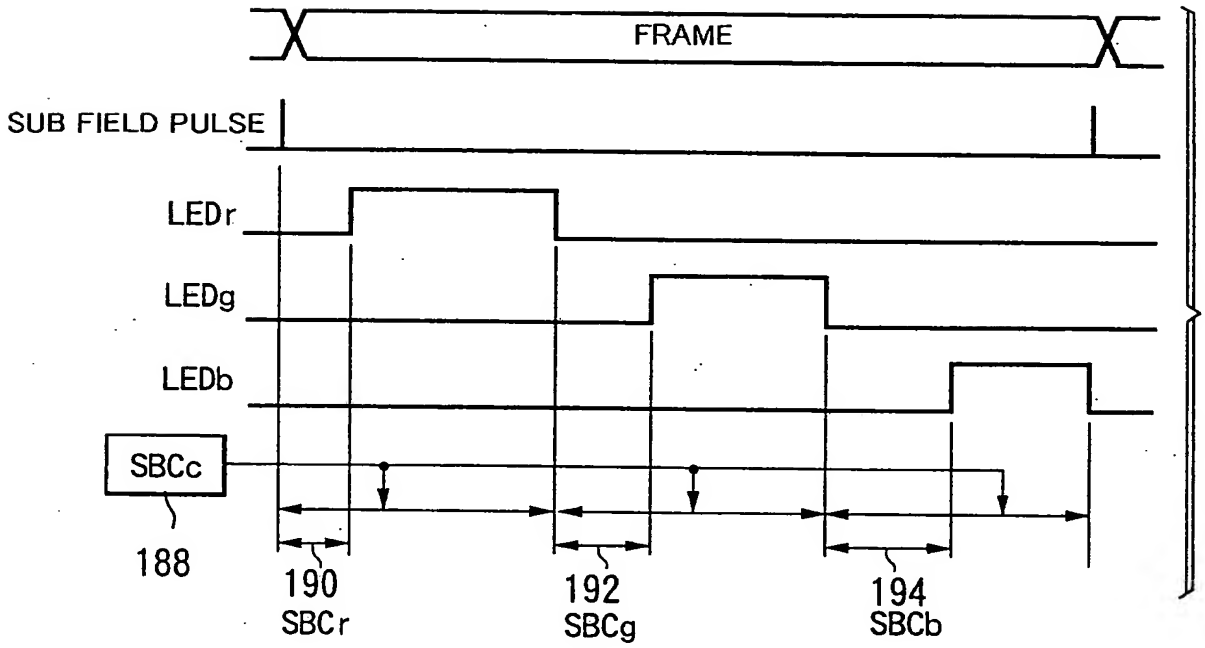
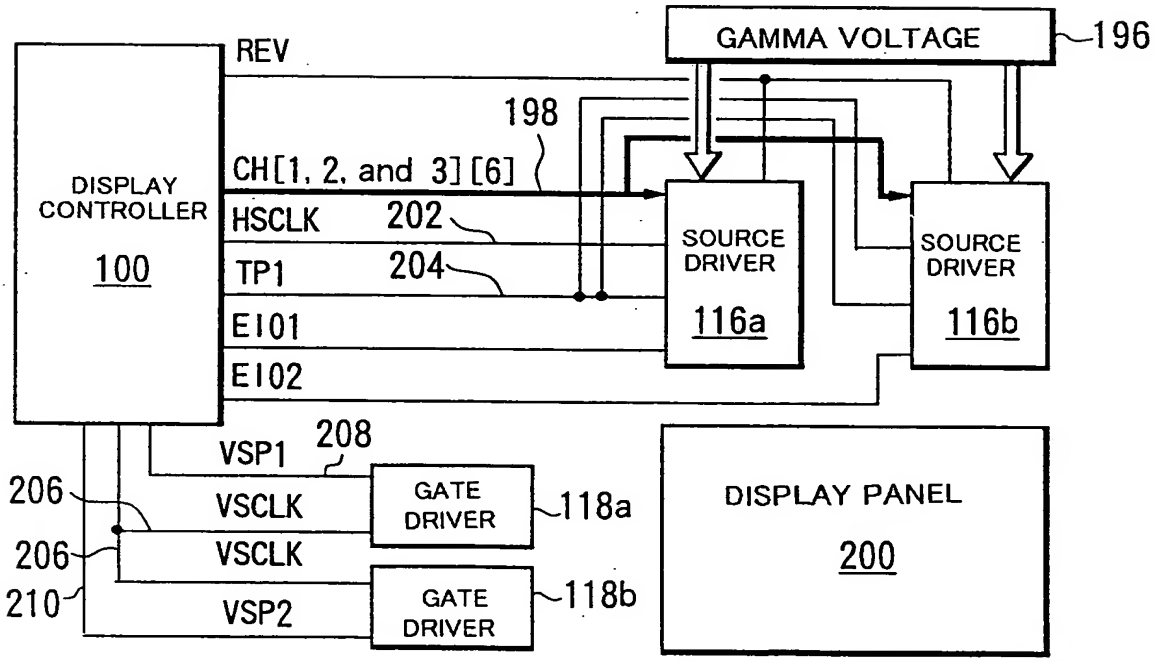

FRAME
SUB FIELD PULSE
LEDr
LEDg
LEDb
SBCc
188
190
SBCr
192
SBCg
194
SBCb

FIG.18


GAMMA VOLTAGE
196
REV
198
CH[1, 2, and 3][6]
DISPLAY CONTROLLER
100
HSCLK
202
TP1
204
EI01
EI02
SOURCE DRIVER
116a
SOURCE DRIVER
116b
VSP1
208
206
VSCLK
GATE DRIVER
118a
206
VSCLK
210
VSP2
GATE DRIVER
118b
DISPLAY PANEL
200

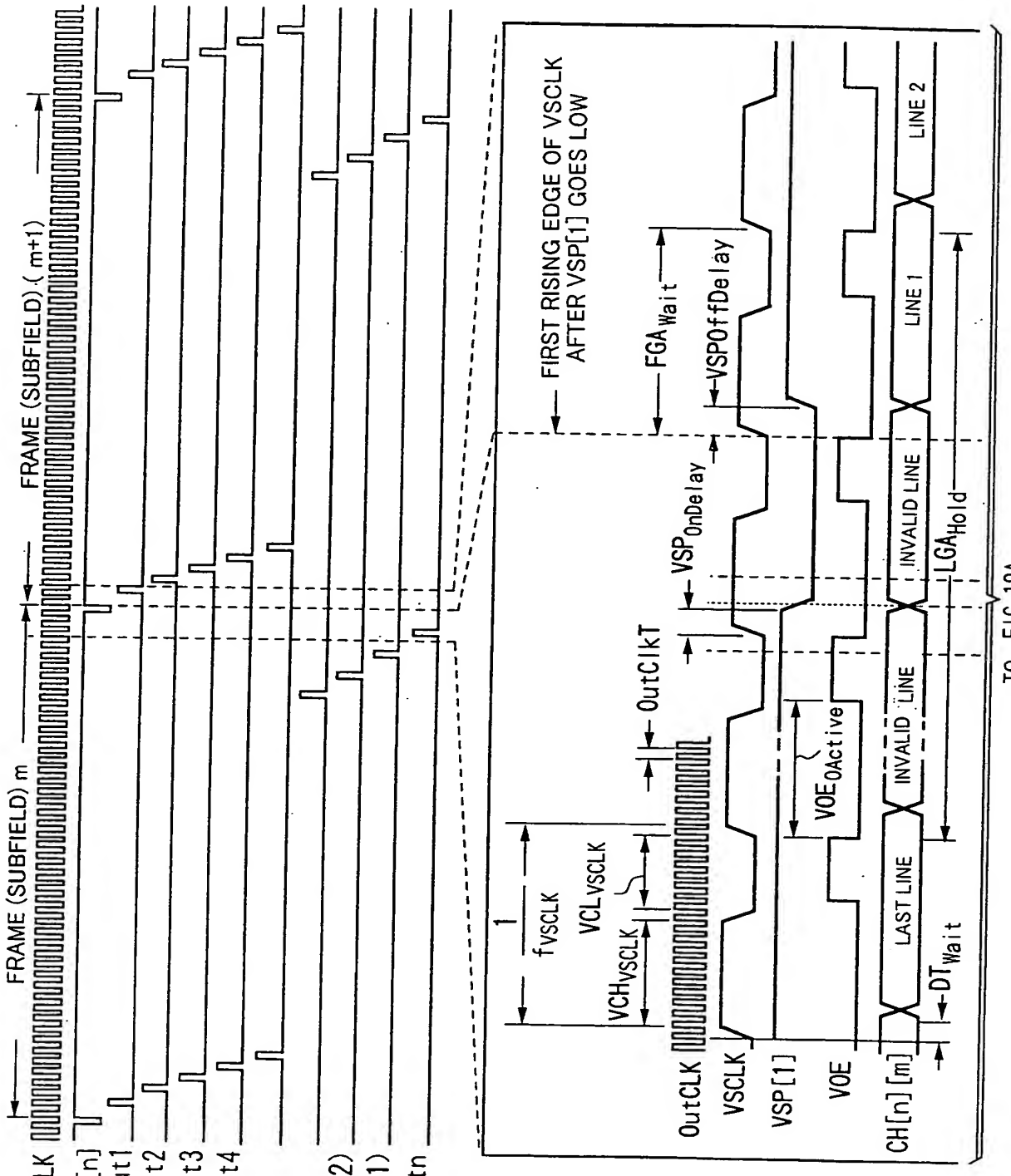

FRAME (SUBFIELD) m
FRAME (SUBFIELD) (m+1)
VSCLK
VSP[n]
Out1
Out2
Out3
Out4
Out(n-2)
Out(n-1)
Outn
FIRST RISING EDGE OF VSCLK AFTER VSP[1] GOES LOW
FGA Wait
VSPOffDelay
VSP OnDelay
OutClkT
1/fVSCLK
VCLVSCLK
VCHVSCLK
VOE OActive
OutCLK
VSCLK
VSP[1]
VOE
CH[n] [m]
LAST LINE
INVALID LINE
INVALID LINE
LINE 1
LINE 2
LGA Hold
DT Wait
TO FIG. 19A

FIG.19A

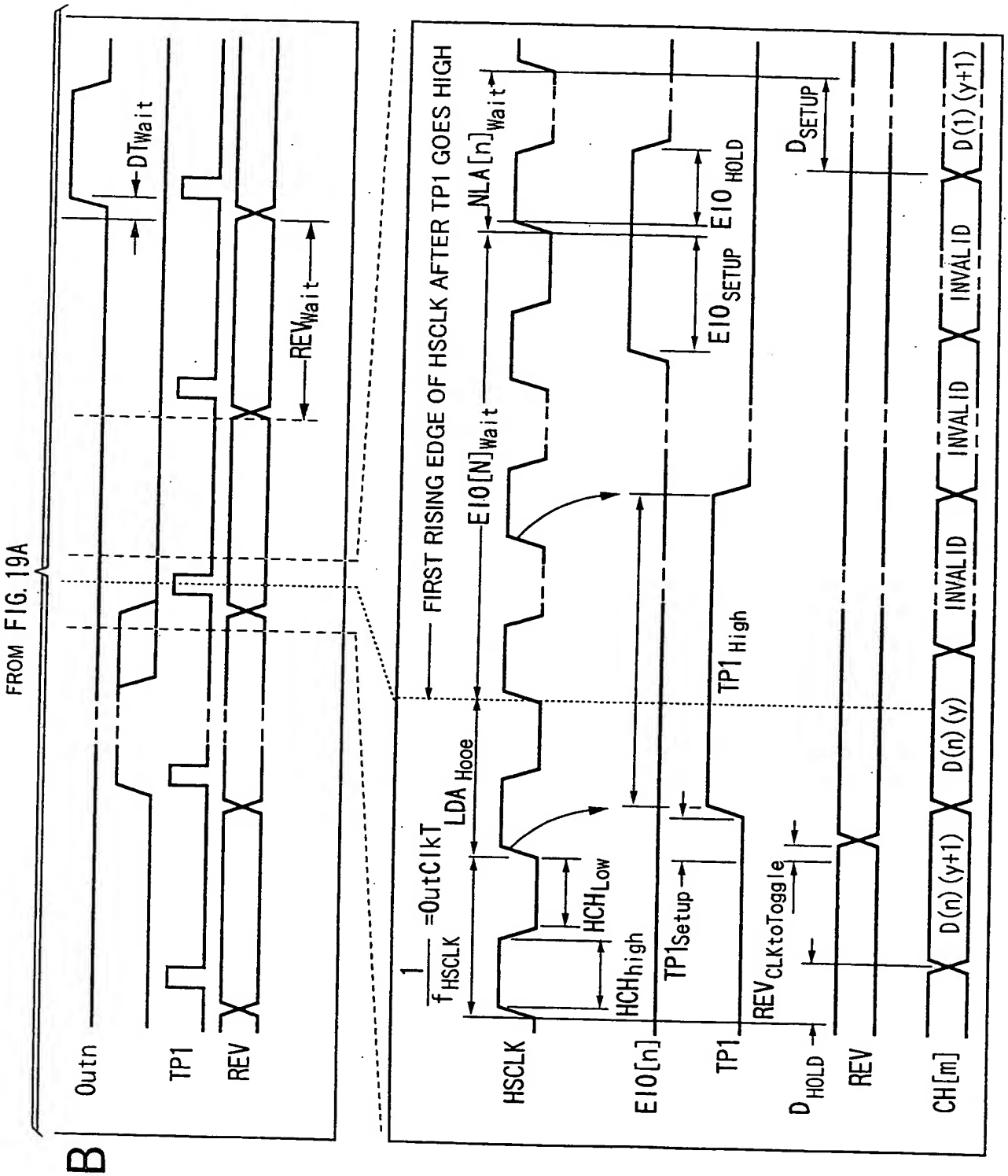

FROM FIG. 19A
Outn
TP1
REV
DTWait
REVWait
FIRST RISING EDGE OF HSCLK AFTER TP1 GOES HIGH
NLA[n]Wait
E10[N]Wait
E10 HOLD
E10 SETUP
DSETUP
1/fHSCLK =OutClkT
LDA Hooe
HCHLow
HCHhigh
TP1Setup
TP1 High
REVCLKtoToggle
HSCLK
E10[n]
TP1
DHOLD
REV
CH[m]
D(n)(y+1)
D(n)(y)
INVALID
INVALID
INVALID
D(1)(y+1)

FIG.19B

FIG.20

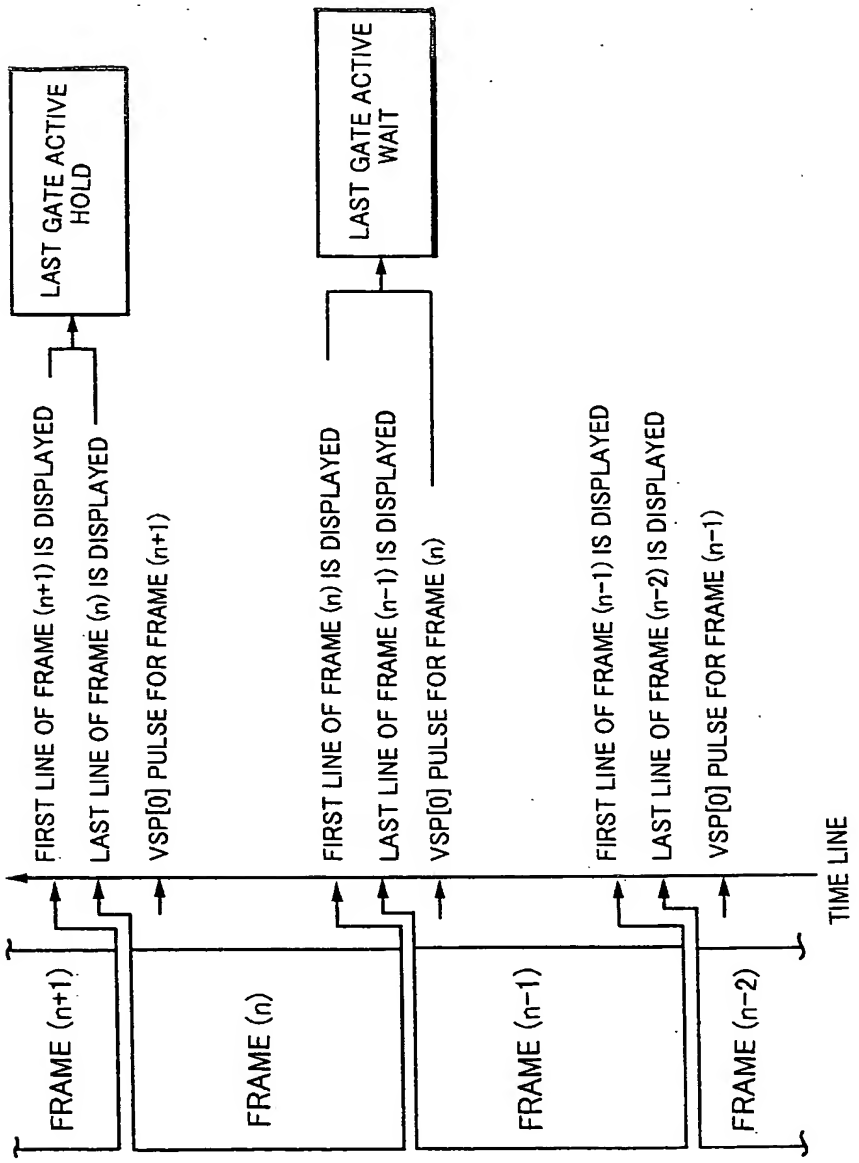

LAST GATE ACTIVE HOLD
LAST GATE ACTIVE WAIT
FIRST LINE OF FRAME (n+1) IS DISPLAYED
LAST LINE OF FRAME (n) IS DISPLAYED
VSP[0] PULSE FOR FRAME (n+1)
FIRST LINE OF FRAME (n) IS DISPLAYED
LAST LINE OF FRAME (n-1) IS DISPLAYED
VSP[0] PULSE FOR FRAME (n)
FIRST LINE OF FRAME (n-1) IS DISPLAYED
LAST LINE OF FRAME (n-2) IS DISPLAYED
VSP[0] PULSE FOR FRAME (n-1)
TIME LINE
FRAME (n+1)
FRAME (n)
FRAME (n-1)
FRAME (n-2)

FIG.21

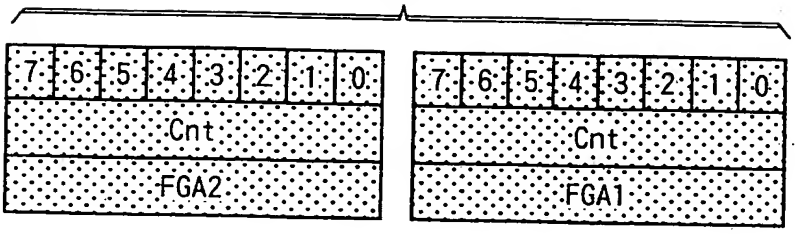


FIG.22

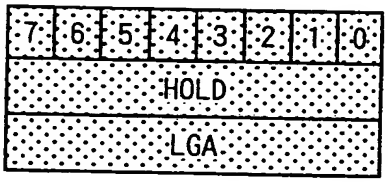


FIG.23

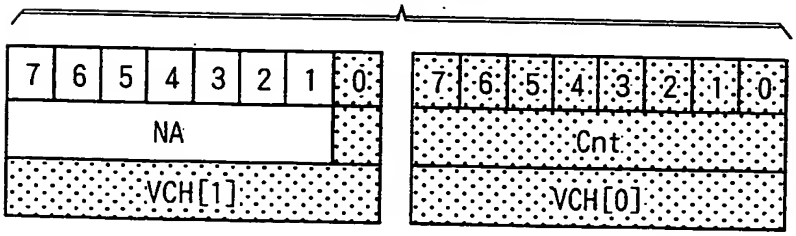


FIG.24

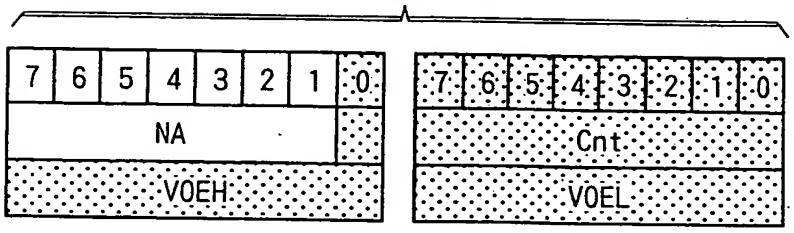


FIG.25

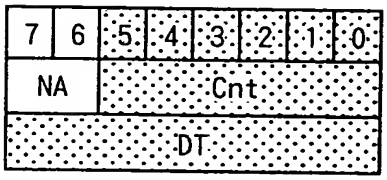


FIG.26

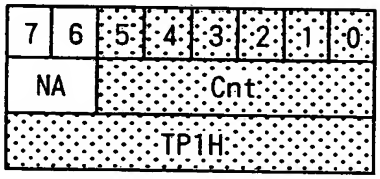


FIG.27

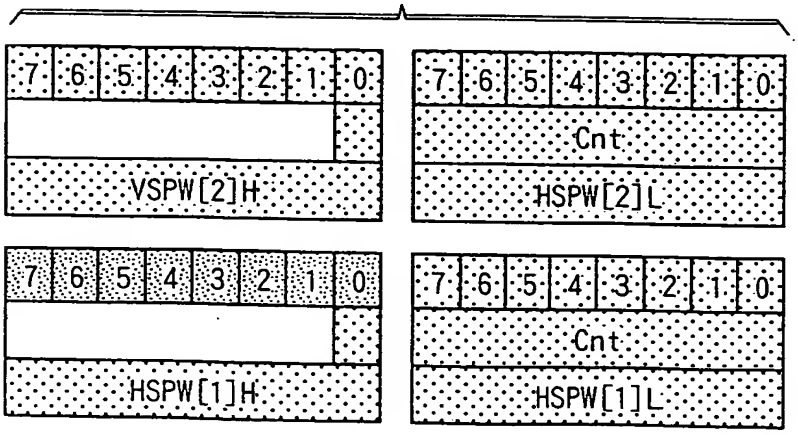


FIG.28

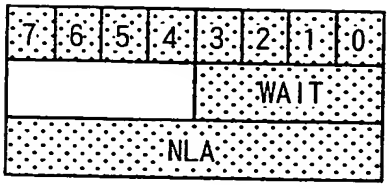


FIG.29

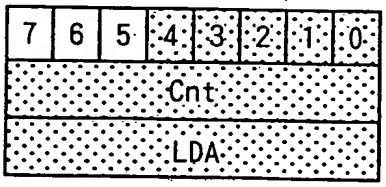


FIG.30

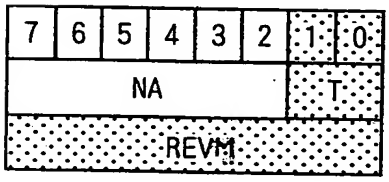


FIG.31

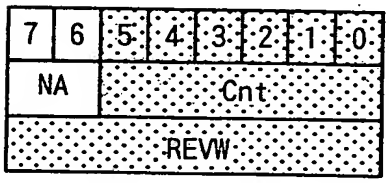


FIG.32

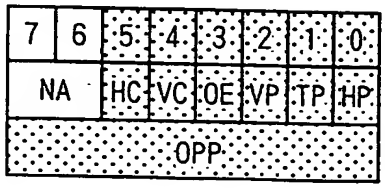
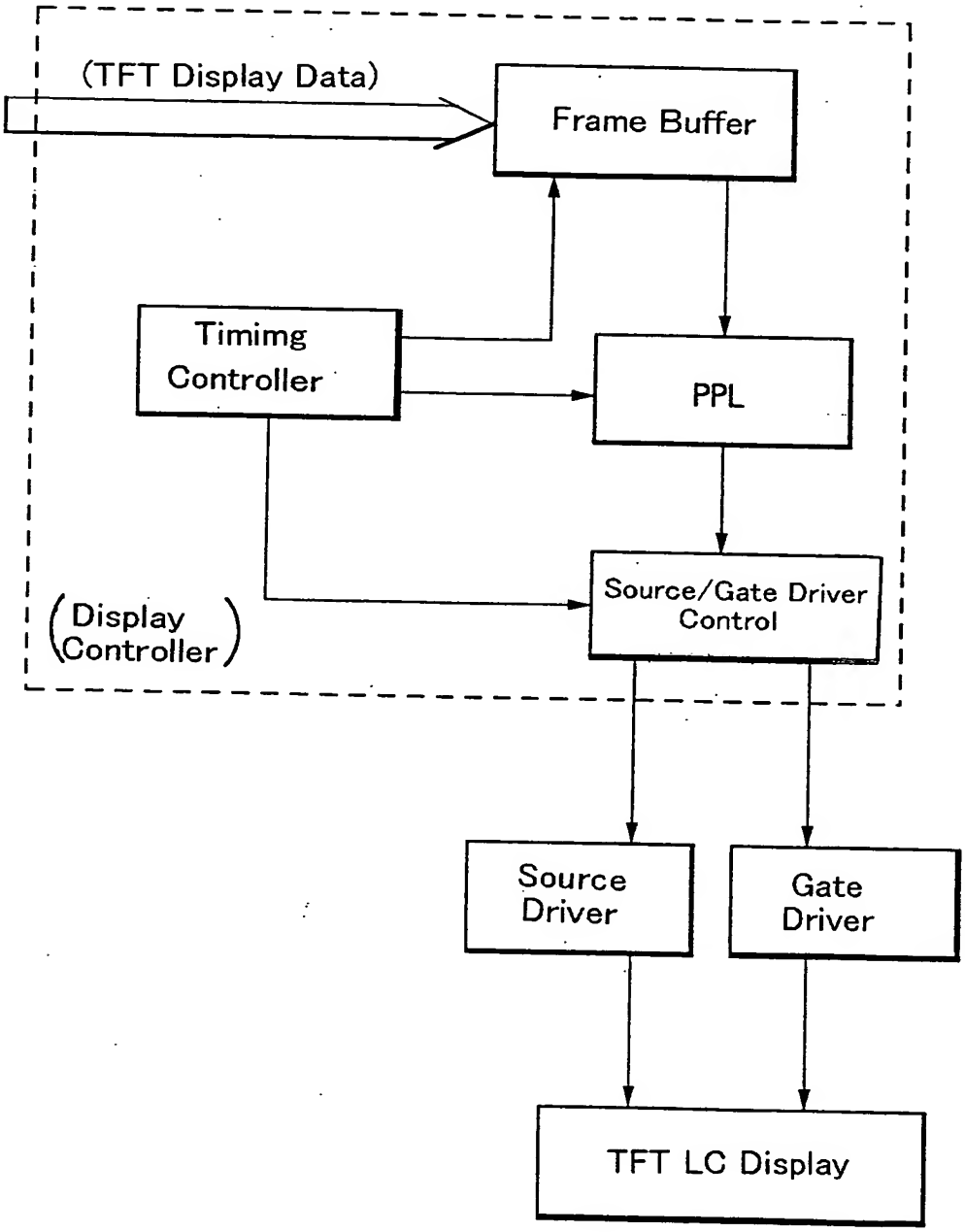


FIG.33


(TFT Display Data)
Frame Buffer
Timimg Controller
PPL
Source/Gate Driver Control
(Display Controller)
Source Driver
Gate Driver
TFT LC Display